

Fig. 3A

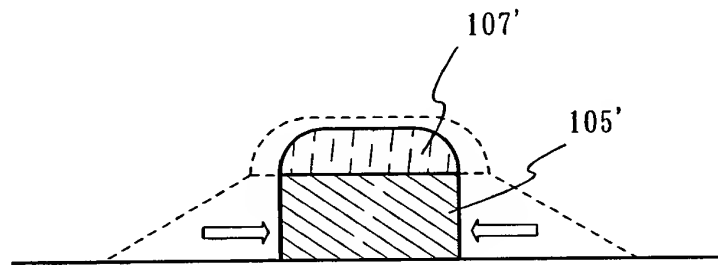


Fig. 3B

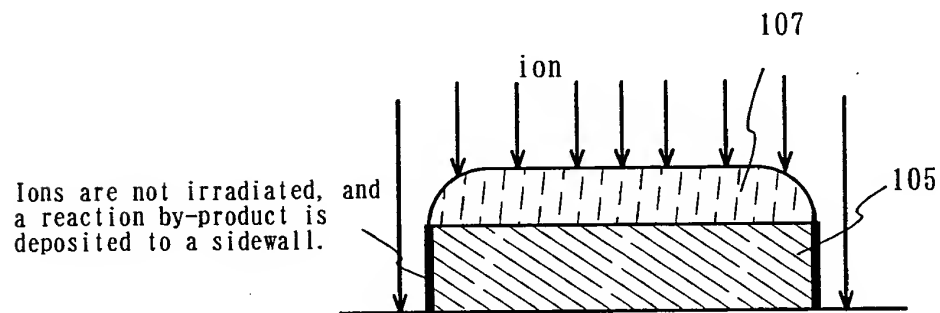


Fig. 4A

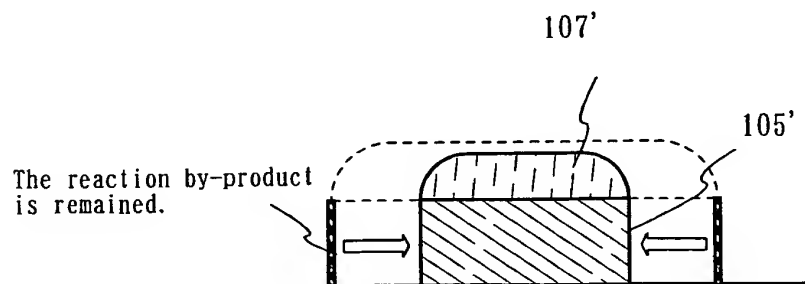


Fig. 4B

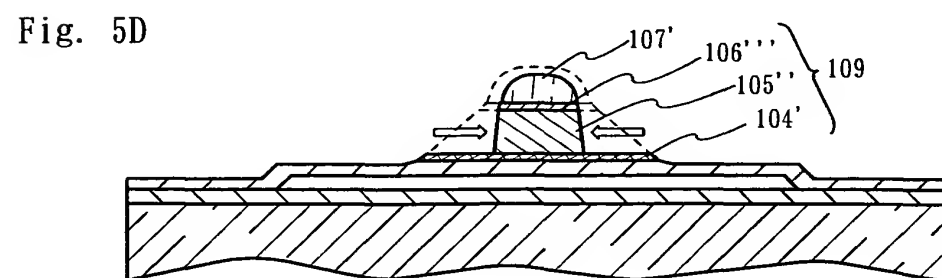
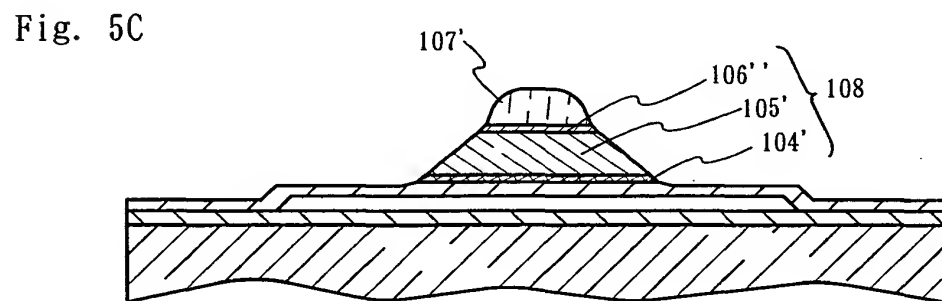
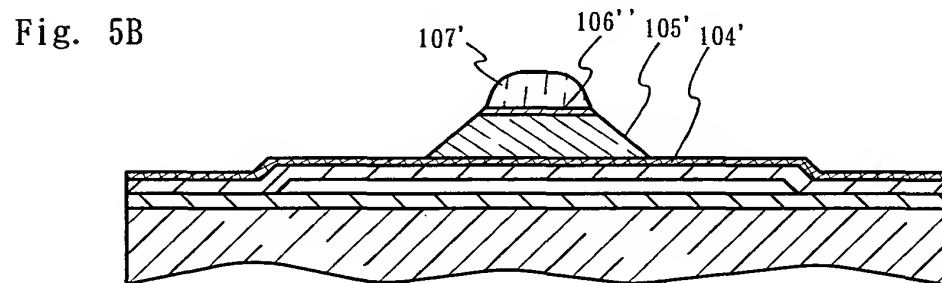
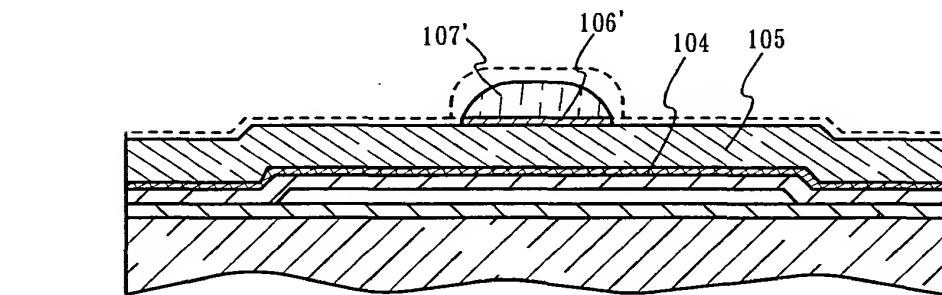
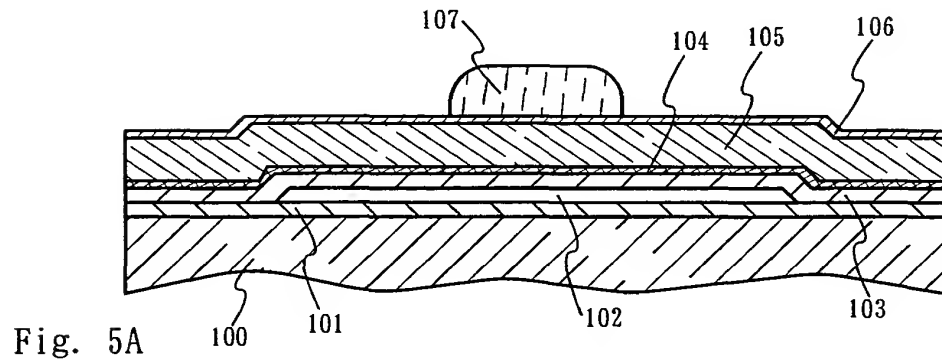


Fig. 5E

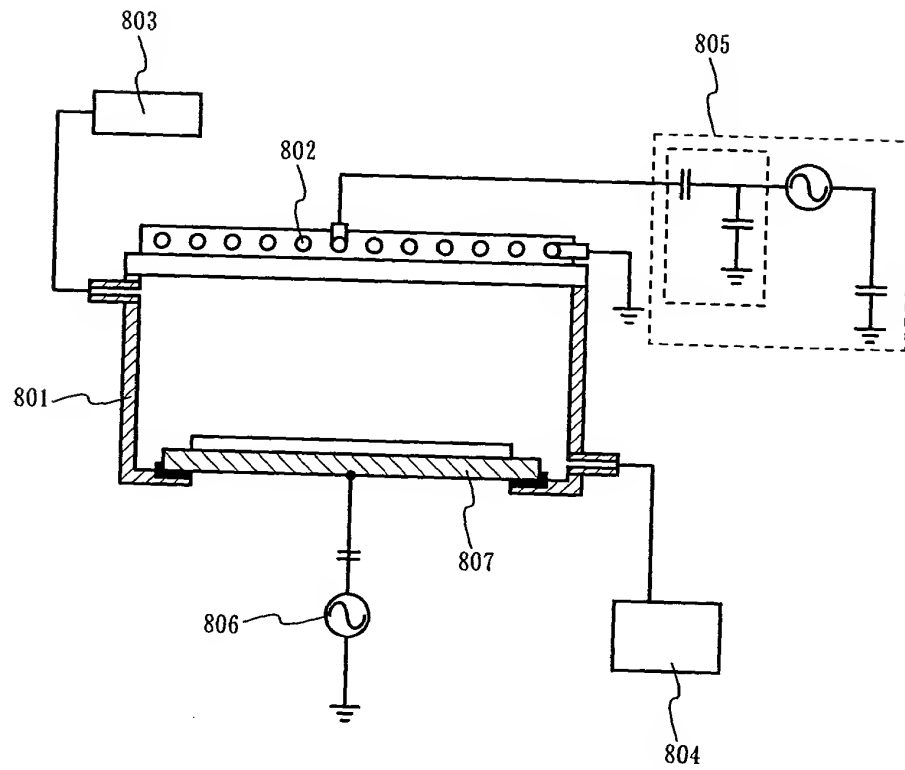


Fig. 6

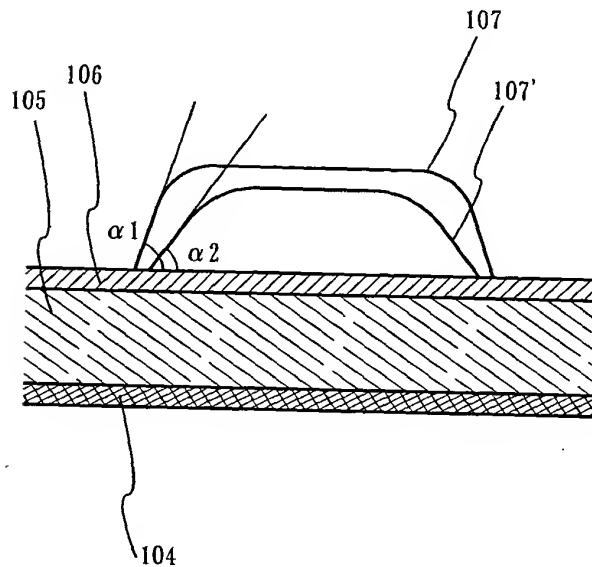


Fig. 7

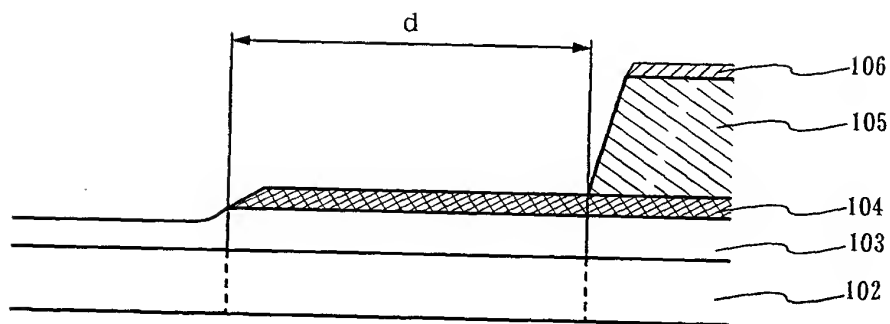
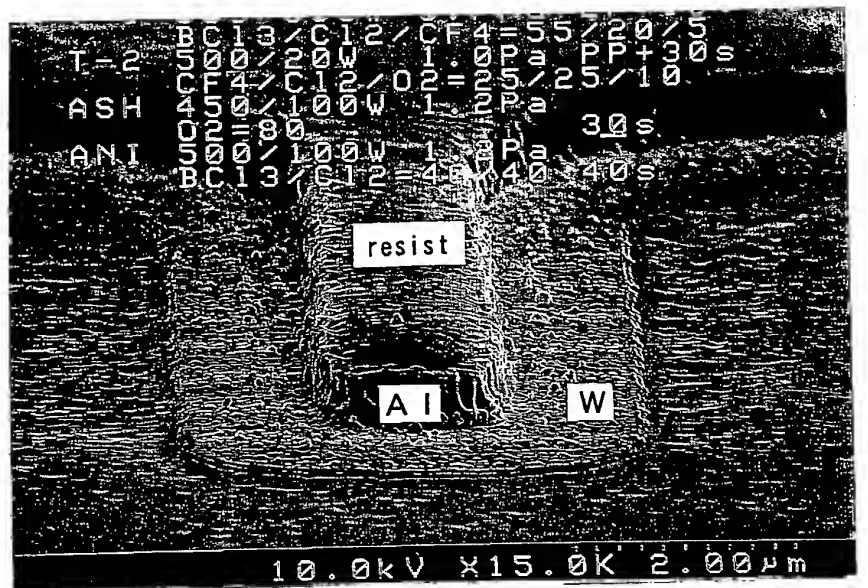


Fig. 8

Applicant(s): Shigeharu Monoe

METHOD FOR MANUFACTURING SEMICONDUCTOR  
DEVICE

2 μm

FIG. 9

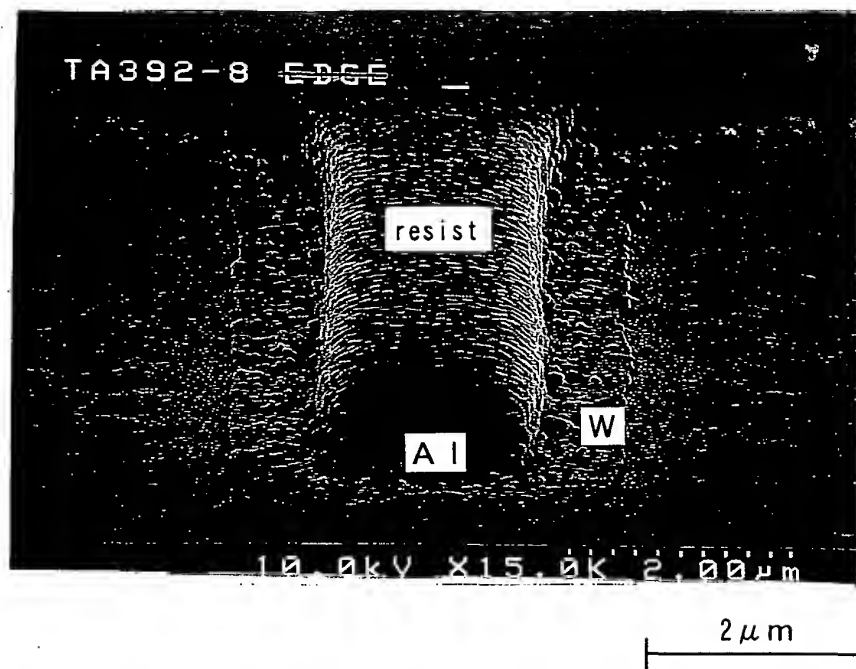


FIG. 10



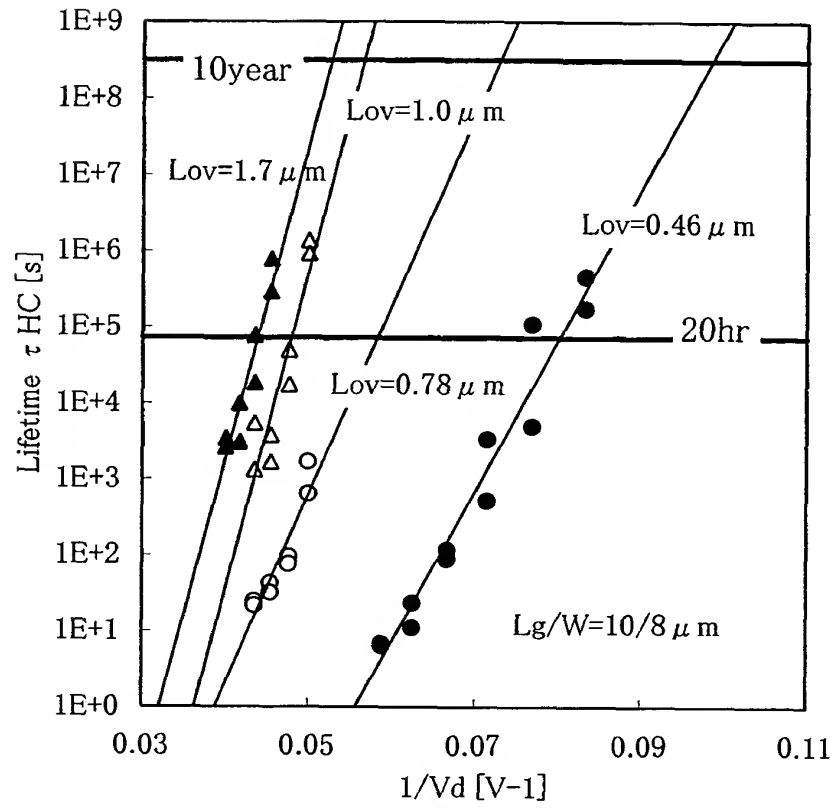


FIG. 11

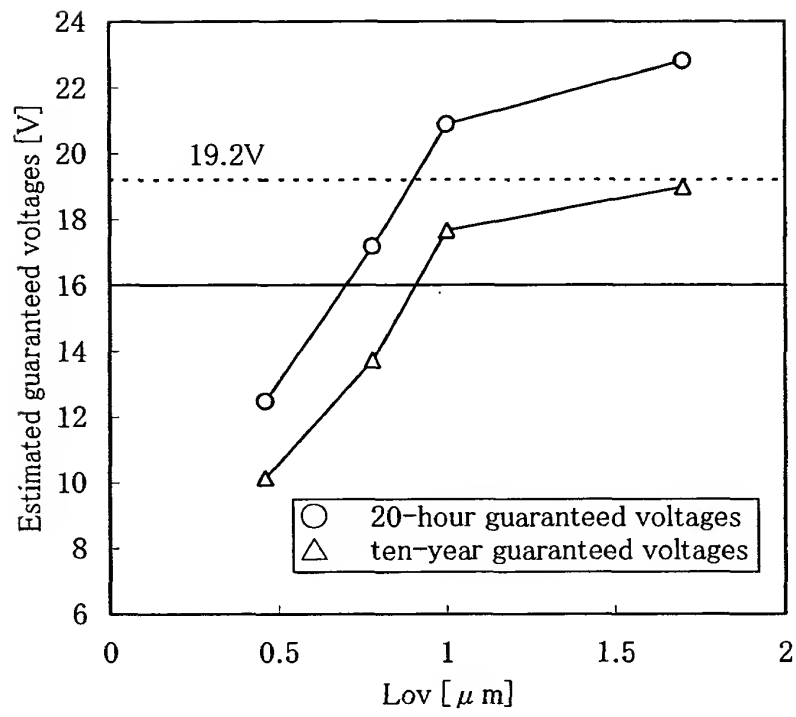


FIG. 12

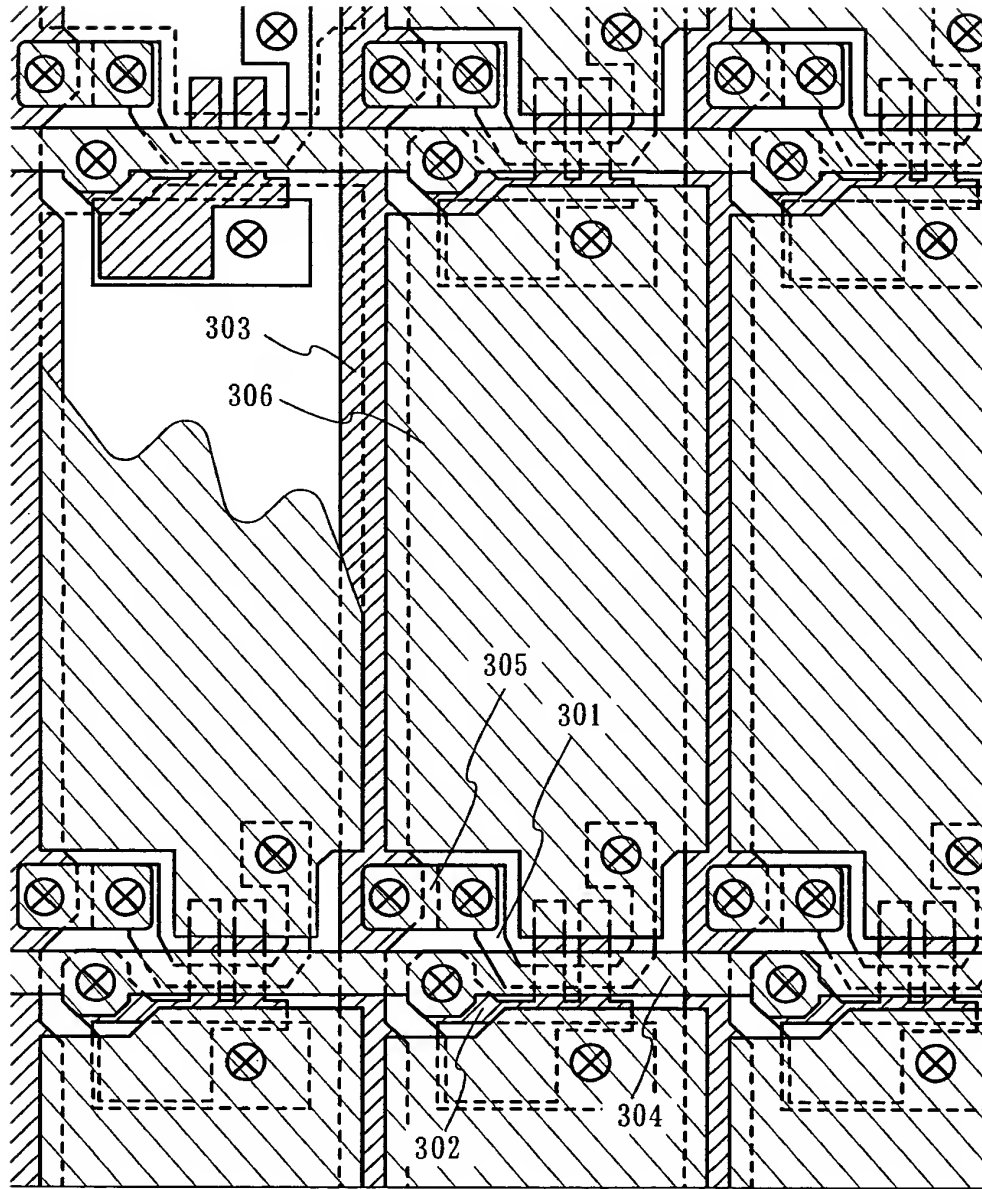


FIG. 13

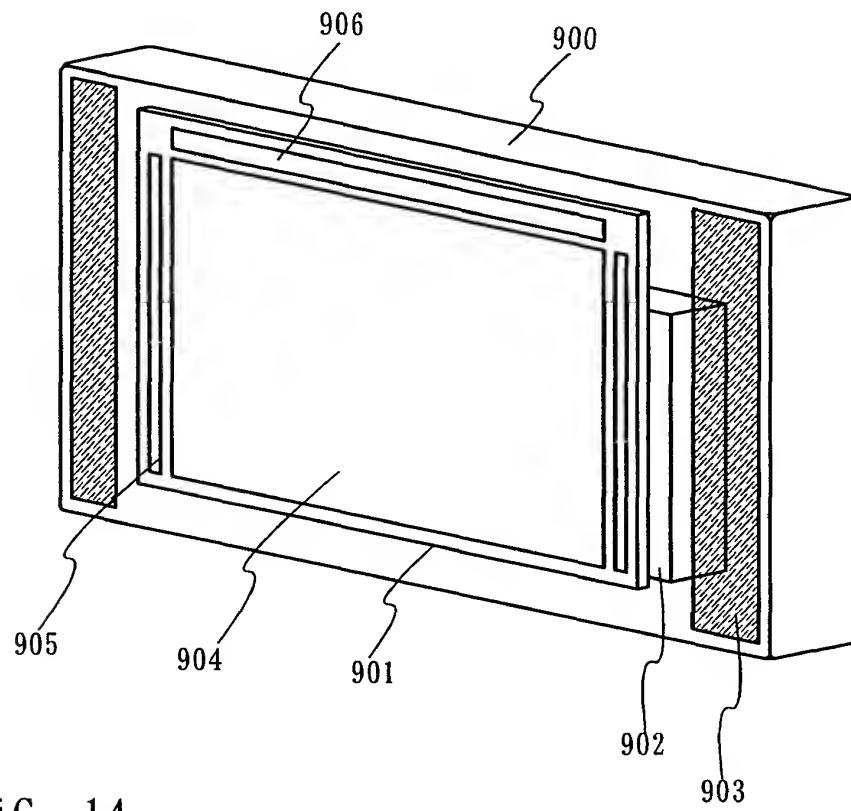


FIG. 14